Die on Carrier, Silicon SPDT Switch, 100 MHz to 60 GHz

FEATURES

- Ultrawideband frequency range: 100 MHz to 60 GHz
- Reflective design
- Bond pads for wire bond and ribbon bond
- Low insertion loss
  - 1.0 dB typical up to 18 GHz
  - 1.3 dB typical up to 44 GHz
  - 1.5 dB typical up to 55 GHz
- High input linearity
  - P1dB: 28 dBm typical
  - IP3: 50 dBm typical
- High RF power handling
  - Through path: 27 dBm up to 40 GHz
  - Hot switching: 27 dBm up to 40 GHz
- No low frequency spurious signals
- RF settling time (50% V_{CTRL} to 0.1 dB of final RF output): 17 ns
- 14-pad, 2.571 mm × 2.471 mm, die on carrier [CHIP]

APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

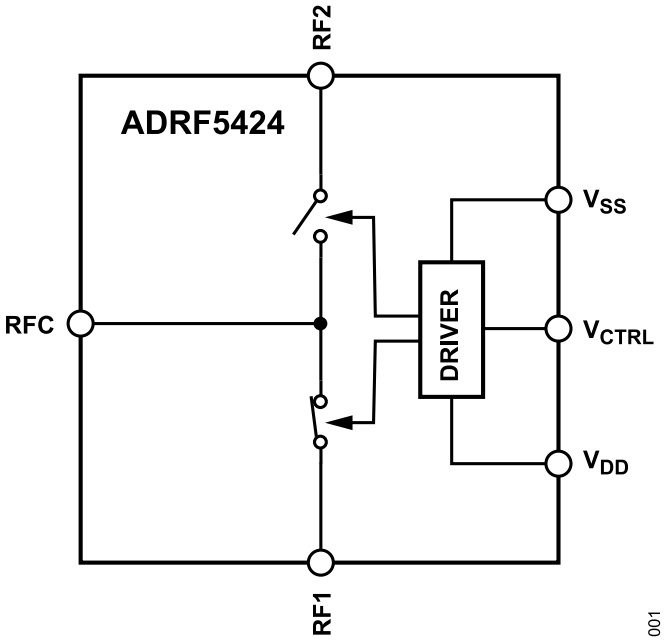


Figure 1.

GENERAL DESCRIPTION

The ADRF5424 is a reflective, single-pole double-throw (SPDT) switch manufactured in a silicon process attached on a gallium arsenide (GaAs) carrier substrate. The substrate incorporates the bond pads for chip and wire assembly, and the bottom of the device is metalized, connected to ground.

This device operates from 100 MHz to 60 GHz with better than 1.5 dB of insertion loss and 35 dB of isolation at 55 GHz. The ADRF5424 has an RF input power handling capability of 27 dBm up to 40 GHz for both the through path and hot switching.

The ADRF5424 draws a low current of 14 µA on the positive supply of +3.3 V and 120 µA on negative supply of −3.3 V. The device features complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5424 is designed to match a characteristic impedance of 50 Ω.

TABLE OF CONTENTS

REVISION HISTORY

2/2024—Rev. A to Rev. B

Changes to Figure 4 and Table 5 ... 7

8/2023—Rev. 0 to Rev. A

Changes to Features Section ... 1
Updated Outline Dimensions ... 12

12/2021—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD}, and T_{DIE} = 25°C for 50 Ω system, unless otherwise noted.

S-parameters are measured with microstrip launchers and 2 mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are deembedded. See Applications Information section for assembly details.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		100		60,000	MHz
INSERTION LOSS					
Between RFC and RF1 or RF2 (On)	100 MHz to 18 GHz		1.0		dB
	18 GHz to 44 GHz		1.3		dB
	44 GHz to 55 GHz		1.5		dB
	55 GHz to 60 GHz		1.9		dB
RETURN LOSS					
RFC and RF1 or RF2 (On)	100 MHz to 18 GHz		15		dB
	18 GHz to 44 GHz		13		dB
	44 GHz to 55 GHz		15		dB
	55 GHz to 60 GHz		15		dB
ISOLATION					
Between RFC and RF1 or RF2 or between RF1 and RF2	100 MHz to 18 GHz		44		dB
	18 GHz to 44 GHz		35		dB
	44 GHz to 55 GHz		35		dB
	55 GHz to 60 GHz		30		dB
SWITCHING CHARACTERISTICS					
Rise and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output		2		ns
On and Off Time (t_{ON} and t_{OFF})	50% V_{CTRL} to 90% of RF output		10		ns
RF Settling Time					
0.1 dB	50% V_{CTRL} to 0.1 dB of final RF output		17		ns
0.05 dB	50% V_{CTRL} to 0.05 dB of final RF output		22		ns
INPUT LINEARITY[1]	Frequency = 200 MHz to 40 GHz				
0.1 dB Power Compression (P0.1dB)					
RFC to RF1 or RF2			27		dBm
RF1 or RF2 to RFC			26		dBm
1 dB Power Compression (P1dB)					
RFC to RF1 or RF2			28		dBm
RF1 or RF2 to RFC			27		dBm
Third-Order Intercept (IP3)	Two tone input power (P_{IN}) = 12 dBm each tone, Δf = 1 MHz		50		dBm
SUPPLY CURRENT	V_{DD} and V_{SS}				
Positive Supply Current (I_{DD})			14		µA
Negative Supply Current (I_{SS})			120		µA
DIGITAL CONTROL INPUTS	V_{CTRL}				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low and High (I_{INL} and I_{INH})			<1		µA
RECOMMENDED OPERATING CONDITONS					
Supply Voltage					
Positive (V_{DD})		3.15		3.45	V

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Negative (V_{SS})		–3.45		–3.15	V
Digital Control Voltage (V_{CTRL})		0		V_{DD}	V
RF Power Handling[2]	Frequency = 200 MHz to 40 GHz, T_{DIE}[3] = 85°C[4]				
Input at RFC					
Through Path	RFC to RF1 or RF2			27	dBm
Hot Switching	RF signal is present at RFC while switching between RF1 and RF2			27	dBm
Input at RF1 or RF2					
Through Path	RF1 or RF2 to RFC			26	dBm
Die Temperature (T_{DIE})[3]		–40		+105	°C

[1] For input linearity performance over frequency, see Figure 13 to Figure 16.

[2] For power derating over frequency, see Figure 2 and Figure 3.

[3] T_{DIE} refers to the bottom of the die on carrier.

[4] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Positive Supply Voltage	–0.3 V to +3.6 V
Negative Supply Voltage	–3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	–0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Power[1] (f = 200 MHz to 40 GHz, T_{DIE} = 85°C[2])	
Input at RFC	
Through Path	27.5 dBm
Hot Switching	27.5 dBm
Input at RF1 or RF2	
Through Path	26.5 dBm
RF Input Power Under Unbiased Condition (V_{DD} and V_{SS} = 0 V)	
Input at RFC	21 dBm
Input at RF1 or RF2	20 dBm
Temperature	
Junction, T_J	135°C
Storage Range	–55°C to +150°C
Processing	170°C

[1] For power derating over frequency, see Figure 2 and Figure 3. This power derating is applicable for insertion loss path and hot switching power specifications.

[2] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specification by 3 dB.

Stresses at or above those listed under absolute maximum ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to carrier bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
C-14-8	352	°C/W

POWER DERATING CURVES

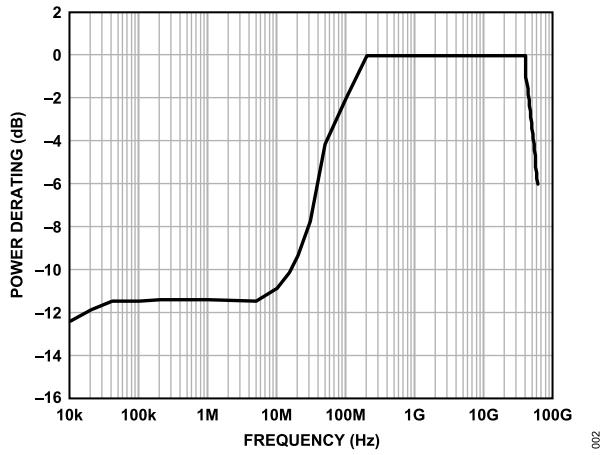


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{DIE} = 85°C

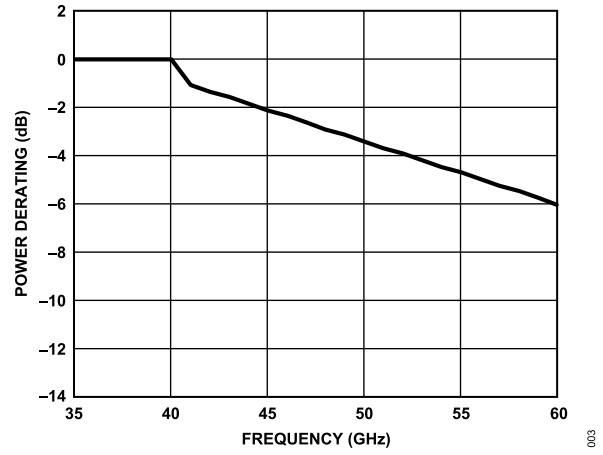


Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{DIE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADRF5424

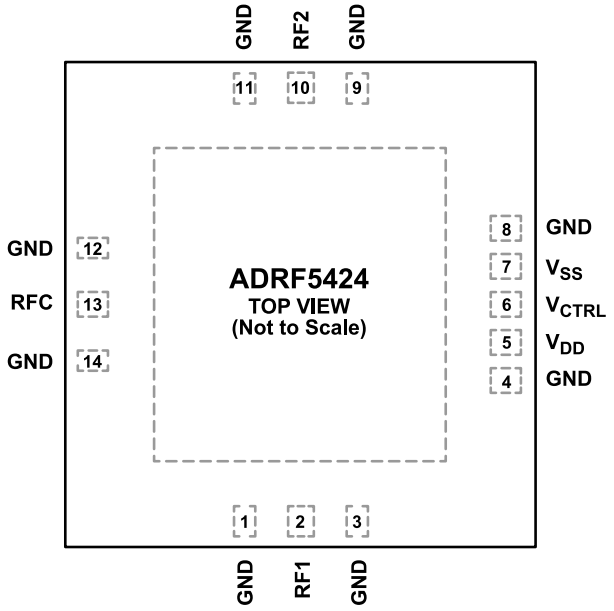
Table 4. ADRF5424, 14-Pad Die on Carrier [CHIP]

ESD Model	Withstand Threshold (V)
Human Body Model (HBM)	
RFC, RF1, and RF2 Pads	±500
Supply and Control Pads	±2000

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE CARRIER BOTTOM IS GOLD METALIZED AND MUST BE DIRECTLY ATTACHED TO THE GROUND PLANE USING CONDUCTIVE EPOXY.

Figure 4. Pad Configuration (Top View)

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 8, 9, 11, 12, 14	GND	Ground. Bonding of these GND pads is optional. See the Applications Information section.
13	RFC	RF Common Port. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
2	RF1	RF Port 1. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
5	V_{DD}	Positive Supply Voltage. See Figure 6 for the interface schematic.
6	V_{CTRL}	Control Input Voltage. See Figure 7 for the interface schematic.
7	V_{SS}	Negative Supply Voltage. See Figure 8 for the interface schematic.
10	RF2	RF Port 2. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
	Carrier Bottom	The carrier bottom is gold metalized and must be directly attached to the ground plane using conductive epoxy.

INTERFACE SCHEMATICS

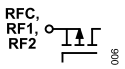


Figure 5. RFC, RF1, RF2 Interface Schematic

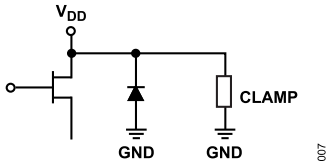


Figure 6. V_{DD} Interface Schematic

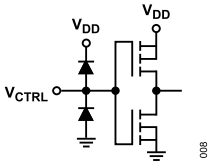


Figure 7. V_{CTRL} Interface Schematic

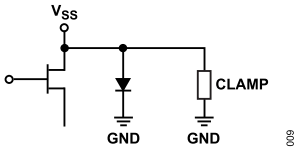


Figure 8. V_{SS} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = –3.3 V, V_{CTRL} = 0 V or V_{DD}, and T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

S-parameters are measured with microstrip launchers and 2 mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are deembedded. See Applications Information section for assembly details.

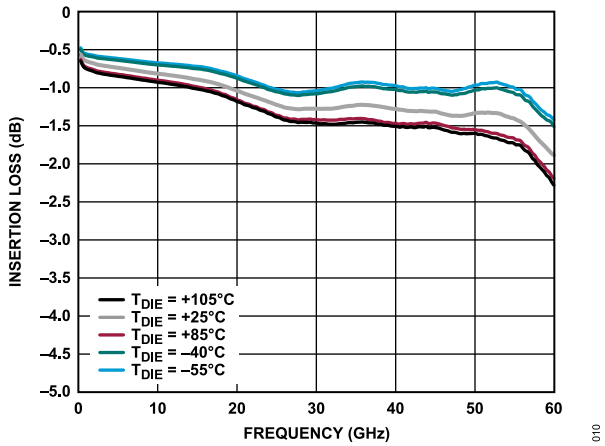


Figure 9. Insertion Loss vs. Frequency over Temperature

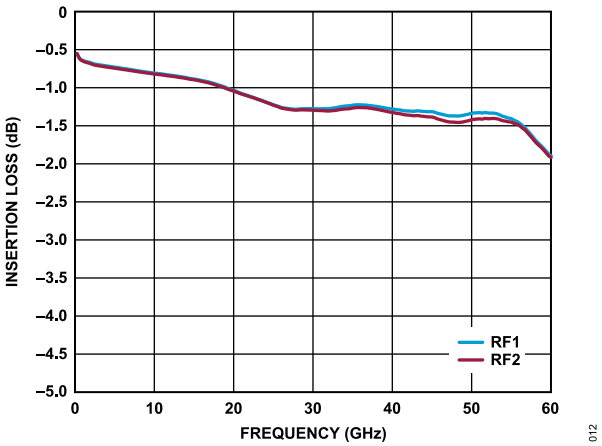


Figure 11. Insertion Loss vs. Frequency for RF1 and RF2

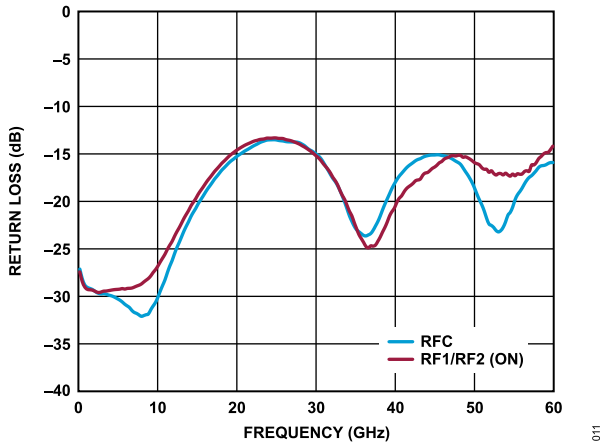


Figure 10. Return Loss vs. Frequency for RFC and RFx (On)

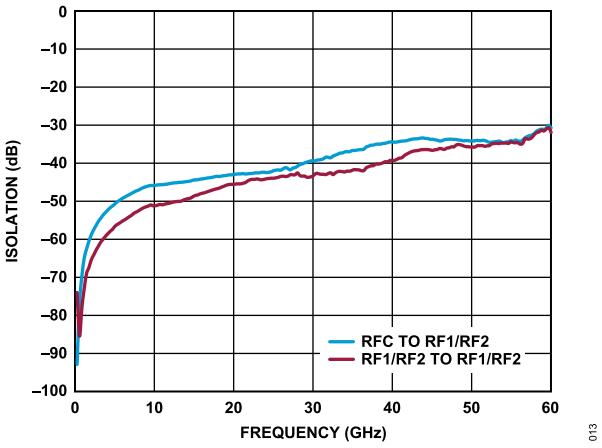


Figure 12. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD}, and T_{DIE} = 25°C for a 50 Ω system, unless otherwise noted.

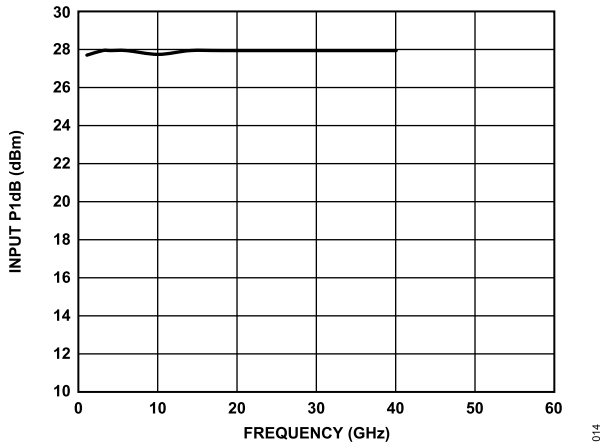


Figure 13. Input P1dB vs. Frequency

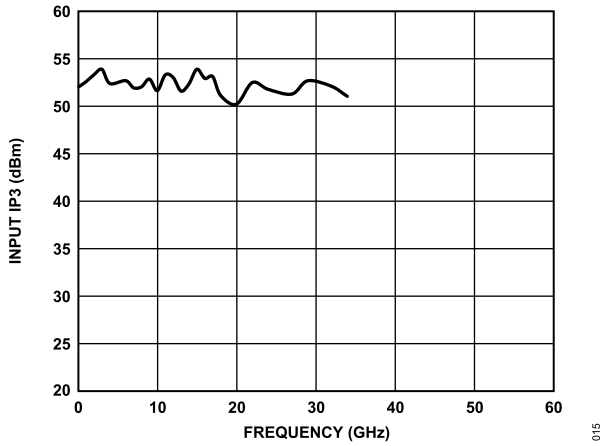


Figure 14. Input IP3 vs. Frequency

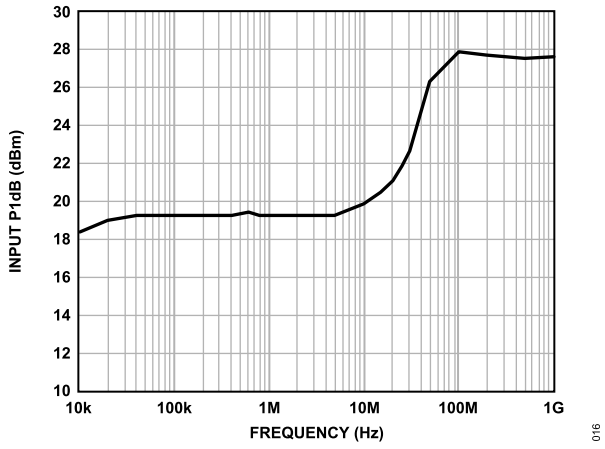


Figure 15. Input P1dB vs. Frequency (Low Frequency Detail)

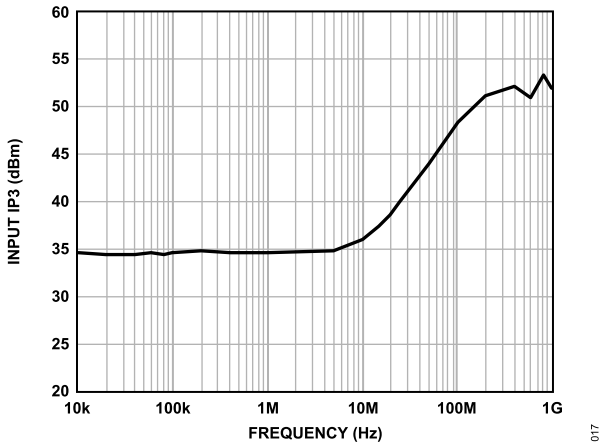


Figure 16. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5424 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS-/LVTTL-compatible control interface. This driver features a single digital control input pad, V_{CTRL}. The logic level applied to the V_{CTRL} pad determines which RF port is in the insertion loss state and in the isolation state (see Table 6). The unselected RF port of the ADRF5424 is reflective. The isolation path provides high isolation between the unselected port and the insertion loss path.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, and RF2) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

POWER SUPPLY

The ADRF5424 requires a positive supply voltage applied to the V_{DD} pad and a negative supply voltage applied to the V_{SS} pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect to GND.
2. Power up the V_{DD} and V_{SS} voltages. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pad. Use pull-up or pull-down resistors if the controller output is in a high impedance state after the V_{DD} voltage is powered up and the control pads are not driven to a valid logic state.
4. Apply an RF input signal to RFC, RF1, or RF2.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 6. Control Voltage Truth Table

	RF Path	
Digital Control Input (V_{CTRL})	**RF1 to RFC**	**RF2 to RFC**
Low	Isolation (off)	Insertion loss (on)
High	Insertion loss (on)	Isolation (off)

APPLICATIONS INFORMATION

DIE ASSEMBLY

An assembly diagram of the ADRF5424 is shown in Figure 17.

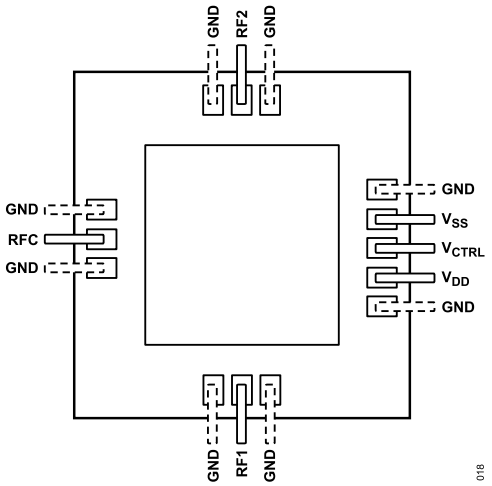


Figure 17. Die Assembly Diagram

The ADRF5424 is designed to have the optimum RF input and output impedance match with 2 mil x 0.5 mil gold ribbon wire and typical 3 mil loop height. The bonding diagrams are shown in Figure 18 and Figure 19. Alternatively, using multiple wire bonds with equivalent inductance yields similar performance. For RF routing from the device, coplanar waveguide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad because the device is designed to match internally the recommended ribbon bond. A spacing of 3 mils from the RF transmission line to the device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The dc pads are large enough to accommodate ribbon bonds, if preferred.

All bonds must be thermosonically bonded at a nominal stage temperature of 150°C, and a minimum amount of ultrasonic energy must be applied to achieve reliable bonds.

The device is metalized on the backside, and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional but still recommended to ensure a solid ground connection.

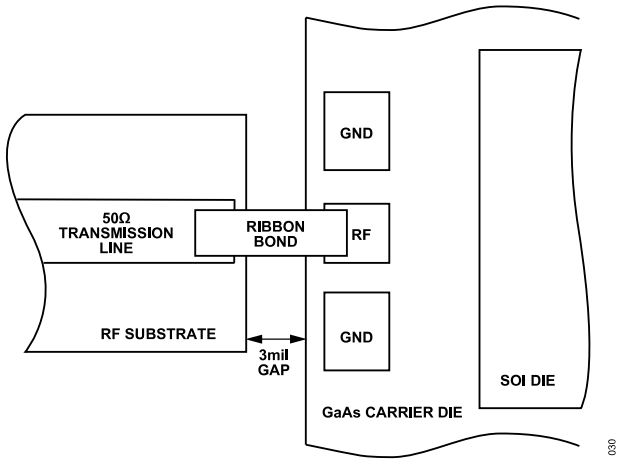


Figure 18. Bonding Diagram Top View

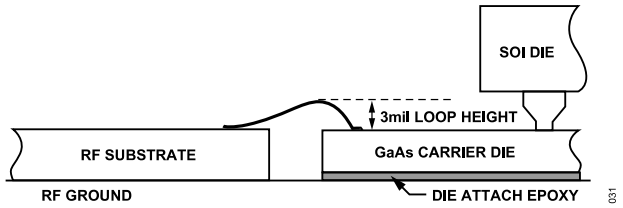


Figure 19. Bonding Diagram Side View

HANDLING, MOUNTING, AND EPOXY DIE ATTACH

Keep devices in ESD protective sealed bags for shipment, and store all bare die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs devices. However, for die on carrier devices, the use of a vacuum tool is recommended to avoid any damage on the device substrate. Handle these devices in a clean environment.

To attach the die with epoxy, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Set epoxy cure temperatures per the recommendations of the manufacturer and the maximum ratings of the device to minimize accumulated mechanical stress after assembly.

Because both dies are attached with solder joints, users must follow best practices for the thermomechanical design of their module assemblies. The temperature expansion coefficient of the substrate material must match the thermal expansion coefficient of the GaAs and silicon (Si) die. Do not allow warpage or other mechanical deformation on the substrate. Set the die attach process and the epoxy cure temperatures to lower the accumulated stress after assembly.

OUTLINE DIMENSIONS

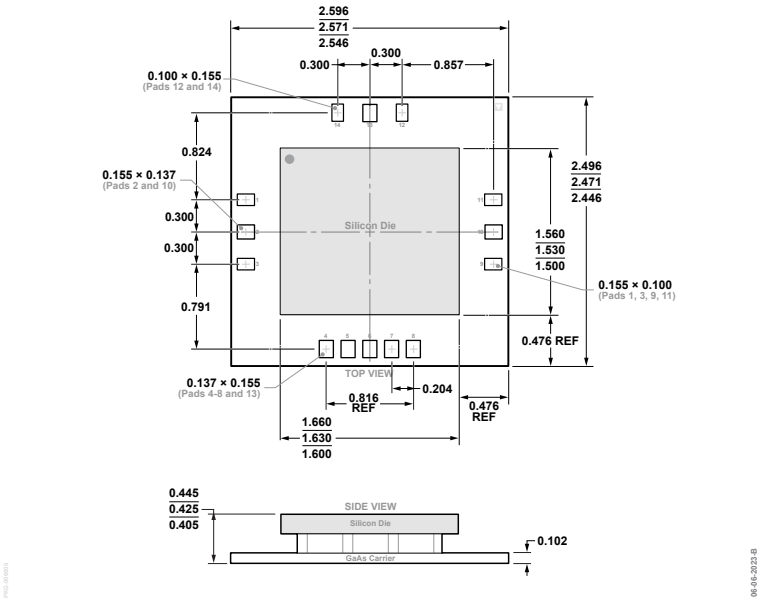


Figure 20. 14-Pad Die on Carrier [CHIP],
(C-14-8),
Dimensions shown in millimeters

Updated: August 19, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5424BCZ	−40°C to +105°C	CHIPS OR DIE	C-14-8
ADRF5424BCZ-GP	−40°C to +105°C	CHIPS OR DIE	C-14-8
ADRF5424BCZ-SX	−40°C to +105°C	CHIPS OR DIE	C-14-8

[1] Z = RoHS Compliant Part.